Sub Q15

1. A method comprising:

receiving a machine instruction directing a processor to search a plurality of data elements; and

executing the machine instruction by:

retrieving M data elements in a single fetch cycle;

concurrently comparing the M data elements to a corresponding current extreme value; and

updating a set of references based on the comparisons.

2. The method of claim 1, wherein retrieving the M data elements comprises retrieving the M data elements as a single data quantity containing the M data elements.

3. The method of claim 2, wherein the set of references comprise pointer registers to store addresses for data quantities.

4. The method of claim 1, wherein M = 1.

5. The method of claim 1, wherein M = 2.

6. The method of claim 1, wherein executing the machine instruction further includes:

storing the current extreme values in M accumulators; and

copying the M data elements to the accumulators based on the comparisons.

7. The method of claim 5, wherein concurrently comparing the data elements comprises processing a first data element with a first execution unit of a pipelined processor and processing a second data element with a second execution unit of the pipelined processor.

8. The method of claim 5, wherein concurrently comparing the data elements comprises concurrently processing a first data element and a second data element within a single execution unit of a pipelined processor.

9. The method of claim 1, wherein concurrently comparing each of the data elements to a current extreme value includes determining whether each of the data elements is less than the corresponding current extreme value.

10. The method of claim 1, wherein concurrently comparing each of the data elements to a current extreme value includes determining whether each of the data elements is greater than the corresponding current extreme value.

11. A method for searching an array of N data elements for a value comprising:

issuing N/M machine instructions to a processor, wherein the processor is adapted to process M data elements in parallel; and

analyzing results of the machine instructions to identify a value for the array.

12. The method of claim 11, further comprising:
executing each machine instruction by:
retrieving M data elements in a single fetch cycle,
concurrently comparing each of the M data elements to a corresponding current extreme value, and
updating the references based on the comparisons.

Q15 Cont'd.

13. A method comprising:
retrieving the pair of data elements from an array of elements in a single fetch operation, wherein the pair of data elements includes an even data element and an odd data element;
substantially comparing the even element of the pair and the odd element of the pair; and
substantially fetching and comparing the remaining pairs of data elements of the array until all of the data elements of the array have been processed.

14. The method of claim 13, wherein substantially comparing the pair of data elements includes setting an even minimum value as function of the even element of the element pair and setting an odd minimum value as function of the odd element of the element pair.

15. The method of claim 13, wherein substantially comparing the pair of data elements includes maintaining a first accumulator to store a minimum value for the even

elements and a second accumulator to store a minimum value for the odd elements.

16. The method of claim 13, further including maintaining a first pointer register to store an address for the minimum value of the even data elements and maintaining a second pointer register to store an address for the minimum value of the odd data elements.

17. The method of claim 16, further including adjusting at least one of the pointer registers after processing all of the pairs of data elements to account for a number of stages in the pipeline.

18. The method of claim 13, wherein the method is invoked by issuing N/M machine instructions to a programmable processor, wherein N equals the number of elements in the array and M equals the number of data elements that the processor can concurrently compare.

19. An apparatus comprising:

a pipeline adapted to process M data elements in parallel; and

a control unit adapted to direct the execution pipeline to search an array of N data elements in response to N/M machine instructions.

20. The apparatus of claim 19, wherein in response to the machine instructions, the control unit directs the pipeline to retrieve M data elements from the array of elements in a

single fetch operation and concurrently compare the data elements to a corresponding current extreme value.

21. The apparatus of claim 19, wherein the pipeline includes M registers adapted to store references to the extreme values.

22. The apparatus of claim 21, wherein the registers are pointer registers.

23. The apparatus of claim 21, wherein the registers are general-purpose data registers.

24. The apparatus of claim 18, wherein the pipeline includes M accumulators to store M current extreme values.

25. The apparatus of claim 18, wherein the pipeline includes M general-purpose registers to store M current extreme values.

26. An article comprising a medium having computer-executable instructions stored thereon for compiling a software program, wherein the computer-executable instructions are adapted to generate N/M machine instructions to search an array of N data elements, each machine instruction causing a programmable processor to:

retrieve M data elements from an array of N elements in a single fetch operation; and

sustantially compare each of the M data elements to a corresponding current extreme value.

27. The article of claim 26, wherein each machine instruction causes the processor to update a set of references based on the comparisons.

28. The article of claim 26, wherein each machine instruction causes the processor to concurrently process a first data element and a second data element within a single execution unit of a pipelined processor.

Cont'd.

29. A system comprising:

a memory device; and

a processor coupled to the memory device, wherein the processor includes a pipeline configured to process M data elements in parallel and a control unit configured to direct the pipeline to search an array of N data elements in response to N/M machine instructions.

30. The system of claim 29, wherein in response to each machine instructions, the control unit directs the pipeline to retrieve M data elements from the array of elements in a single fetch operation and concurrently compare the data elements to a corresponding current extreme value.

31. The system of claim 29, wherein the pipeline includes M registers configured to store references to the extreme values.

32. The system of claim 31, wherein the registers are pointer registers.

Q15 cont.

33. The system of claim 31, wherein the registers are general-purpose data registers.

34. The system of claim 29, wherein the memory device comprises static random access memory.

35. The system of claim 29, wherein the memory device comprises FLASH memory.